CLAIMS

1. A data transfer controller connecting a high-speed bus having a relatively high data transfer rate to a low-speed bus having a relatively low data transfer rate, the controller comprising:

an address register for storing an address allotted to a peripheral device connected to the low-speed bus, the stored address being referred to as a preset address;

a buffer for storing a data retrieved from the peripheral device based on the preset address, the retrieved data being referred to as prefetched data; and

a central controller for causing the prefetched data stored in the buffer to be outputted into the high-speed bus when a peripheral device address transmitted through the high-speed bus is identical to the preset address.

- 2. The data transfer controller according to claim 1, wherein the address register holds an address having relatively high access frequency.
- 3. The data transfer controller according to claim 1, wherein the high-speed bus and the low-speed bus are arranged within a computer.

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4. The data transfer controller according to claim 1, wherein the high-speed bus is arranged within a computer, the low-speed bus being a cable arranged outside of the

computer.

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5. A method of transferring data between a high-speed bus having a relatively high data transfer rate and a low-speed bus having a relatively low data transfer rate, the method comprising the steps of:

storing an address allotted to a peripheral device connected to the low-speed bus, the stored address being referred to as a preset address;

storing a data retrieved from the peripheral device based on the preset address, the retrieved data being referred to as prefetched data; and

causing the stored prefetched data to be outputted into the high-speed bus when a peripheral device address transmitted through the high-speed bus is identical to the preset address.